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Pat. No. 06004754 - 5
Issue Date: 08/30/04

Group ID: D
User ID: SXHolt
Page 1
KS: 12,523

Warning [Pages Of US References:]

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page 9 has no references
page 10 has no references
page 11 has no references
page 12 has no references

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characters are the same as position 2 on page 12

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Rule 47 Continuing Data PCT Disclaimer

No ADS No Yes —

Microfiche Appendix CPA tag

No No —

Foreign Priority Claimed: No —

Acknowledged: No

Text Endorsement: 10086197.030102

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JACKET

<u>SERIAL NUMBER</u>	<u>FILING DATE</u>	<u>CLASS</u>	<u>SUBCLASS</u>	<u>GAU</u>
10/086,197	03/01/02	712	23	2154

FOREIGN PRIORITY
Country Document Number Date —

DISCLAIMER

/ /

TITLE

Superscalar RISC instruction scheduling

MICROFICHE APPENDIX

ASSISTANT EXAMINER:

First: Middle: Last:

PRIMARY EXAMINER:

First: Middle: Last:

Larry D. Donaghue —

CLAIMS ALLOWED
Total Print

19 1

DRAWINGS

Sheets Figures Print

9 11 Y

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BLUE SLIP INFORMATION

<u>SERIAL NUMBER</u>	<u>CLASS</u>	<u>SUBCLASS</u>	<u>GAU</u>
10/086,197	712.	23	2154

<u>INDEP. CLAIMS</u>	<u>TOTAL CLAIMS</u>
1,13	19

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BLUE SLIP (Page 1)

INTERNATIONAL CLASSIFICATION

Class SubClass

G06F 9/38

CROSS-REFERENCES

Class SubClass

712 218;216

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TERM EXTENSION

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FIELD OF SEARCH

Class SubClass

712 23;218;217;216

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OATH

INVENTOR NAME

First:

Middle:

Last:

Signed:

Sanjiv

Garg

Yes

City: Freemont

State: CA ZIP Code: Country: Foreign ZIP:

INVENTOR NAME

First: Middle: Last: Signed:

Kevin Ray Iadonato

Yes

City: San Jose

State: CA ZIP Code: Country: Foreign ZIP:

INVENTOR NAME

First: Middle: Last: Signed:

Le Trong Nguyen

Yes

City: Monte Sereno

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INVENTOR NAME

First: Middle: Last: Signed:

Johannes Wang

Yes

City: Redwood City

State: CA ZIP Code: Country: Foreign ZIP:

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PCT INFO
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CONTINUING DATA (Page 1)

<u>LINE</u>	<u>CODE</u>	<u>SERIAL NUMBER</u>	<u>FILING DATE</u>	<u>STATUS</u>	<u>DOCUMENT NO.</u>	<u>ISSUE DATE</u>
104	71	09/906,099	07/17/2001	03		/ /
105	81	09/329,354	06/10/1999	01	6,289,433	/ /

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